Claims

[c1] What is claimed is:

1. A pipelined N-point transform processor comprising:

a first triplet comprising a first butterfly I unit (BFI), a butterfly II unit (BFII) and a butterfly III unit (BFIII) connected together in series, an input port of the first BFI serving as an input port of the triplet to accept complex numbers, an output port of the BFIII serving as an output port of the triplet;

a complex multiplier accepting a complex result from the output port of the first triplet, and accepting a coefficient to generate a complex product;

an output portion comprising at least a second BFI, an input port of the second BFI accepting the complex product from the complex multiplier, the output portion providing output transformed complex numbers; and

a control unit comprising a pipeline step-count register, and means for providing coefficients to the complex multiplier;

wherein the control unit controls each BFI, each BFII, each BFIII, and provides each coefficient, according to a value held in the pipeline step-count register.

[c2] 2. The processor of claim 1 wherein the means for providing coefficients to the complex multiplier includes a table of coefficients stored in the control unit.

[c3] 3. The processor of claim 1 wherein each BFI comprises:

a first first-in-first-out (FIFO) buffer capable of storing at least a complex number;

a first complex adder accepting input from the first FIFO and from the input port of the BFI to generate a resulting first complex sum;

a first complex subtractor accepting input from the first FIFO and from the input port of the BFI to generate a resulting first complex difference;

a first multiplexer as an output port of the BFI, the first multiplexer selecting a value from the first FIFO or the first complex sum from the first complex adder according to a first control line; and

a second multiplexer for providing input to the first FIFO, the second multiplexer selecting a value from the input port of the BFI or the first complex difference from the first complex subtractor according to a second control line;

wherein the first control line and the second control line are driven by the

control unit according to a value held within the pipeline step-count register.

[c4] 4. The processor of claim 3 wherein the first FIFO stores L_1 complex numbers, and for a first L_1 iterations as determined by the pipeline step-count register the control unit controls the first and second control lines to cause the first multiplexer to select the output of the first FIFO and causes the second multiplexer to select the values from the input port of the BFI, and for an immediately subsequent second L_1 iterations as determined by the pipeline step-count register the control unit controls the first and second control lines cause the first multiplexer to select the first complex sum and causes the second multiplexer to select the first complex difference.

[c5] 5. The processor of claim 4 wherein $L_1 = N/(2 \times 8^p)$, where p indicates a triplet number.

[c6] 6. The processor of claim 1 wherein each BFII comprises:

a second first-in-first-out (FIFO) buffer capable of storing at least a complex number;

a first $\pi/2$ complex rotator connected to an input port of the BFII to generate a corresponding first complex $\pi/2$ rotated value;

a third multiplexer for selecting as output an input value from the input port of the BFII or the first complex $\pi/2$ rotated value according to a third control line;

a second complex adder accepting the output from the third multiplexer and from the second FIFO to generate a resulting second complex sum;

a second complex subtractor accepting input from the second FIFO and the output from the third multiplexer to generate a resulting second complex difference;

a fourth multiplexer as an output of the BFII, the fourth multiplexer selecting either a value from the second FIFO or the second complex sum from the second complex adder according to a fourth control line; and

a fifth multiplexer for providing input to the second FIFO, the fifth multiplexer selecting the output of the third multiplexer or the second complex difference from the second complex subtractor according to a fifth control line.

[c7] wherein the third, fourth and fifth control lines are driven by the control unit

according to a value held within the pipeline step-count register.

[c8] 7. The processor of claim 6 wherein the second FIFO stores L_2 complex numbers, and for a first L_2 iterations as determined by the pipeline step-count register the control unit controls the fourth and fifth control lines to cause the fourth multiplexer to select the output of the second FIFO and causes the fifth multiplexer to select the output from the third multiplexer, and for an immediately subsequent second L_2 iterations as determined by the pipeline step-count register the control unit controls the fourth and fifth control lines to cause the fourth multiplexer to select the second complex sum and causes the fifth multiplexer to select the second complex difference.

[c9] 8. The processor of claim 7 wherein $L_2 = N/(4 \times 8^p)$, where p indicates a triplet number.

[c10] 9. The processor of claim 7 wherein the control unit drives the third control line according to a value within the pipeline step-count register to generate coefficients consistent with a transform process.

[c11] 10. The processor of claim 1 wherein each BFIII comprises:

a third first-in-first-out (FIFO) buffer capable of storing at least a complex number;

a second $\pi/2$ complex rotator connected to an input port of the BFIII to generate a corresponding second complex $\pi/2$ rotated value;

a sixth multiplexer for selecting as output an input value from the input port of the BFIII or the second complex $\pi/2$ rotated value according to a sixth control line;

a $\pi/4$ complex rotator connected to the output of the sixth multiplexer to generate a corresponding complex $\pi/4$ rotated value;

a seventh multiplexer for selecting as output the output from the sixth multiplexer or the complex $\pi/4$ rotated value according to a seventh control line;

a third complex adder accepting the output from the seventh multiplexer and from the third FIFO to generate a resulting third complex sum;

a third complex subtractor accepting input from the third FIFO and the output

from the seventh multiplexer to generate a resulting third complex difference;
an eighth multiplexer as an output of the BFIII, the eighth multiplexer selecting either a value from the third FIFO or the third complex sum from the third complex adder according to an eighth control line; and
a ninth multiplexer for providing input to the third FIFO, the ninth multiplexer selecting the output of the seventh multiplexer or the third complex difference from the third complex subtractor according to a ninth control line.

[c12] wherein the sixth, seventh, eighth and ninth control lines are driven by the control unit according to a value held within the pipeline step-count register.

[c13] 11. The processor of claim 10 wherein the third FIFO stores L_3 complex numbers, and for a first L_3 iterations as determined by the pipeline step-count register the control unit controls the eighth and ninth control lines to cause the eighth multiplexer to select the output of the third FIFO and causes the ninth multiplexer to select the output from the seventh multiplexer, and for an immediately subsequent second L_3 iterations as determined by the pipeline step-count register the control unit controls the eighth and ninth control lines to cause the eighth multiplexer to select the third complex sum and causes the ninth multiplexer to select the third complex difference.

[c14] 12. The processor of claim 11 wherein $L_3 = N/(8 \times 8^p)$, where p indicates a triplet number.

[c15] 13. The processor of claim 11 wherein the control unit drives the sixth and seventh control lines according to a value within the pipeline step-count register to generate coefficients consistent with a transform process.

[c16] 14. The processor of claim 10 wherein the $\pi/4$ complex rotator comprises:
a third $\pi/2$ complex rotator for accepting a complex value from an input port of the $\pi/4$ complex rotator and generating a corresponding third $\pi/2$ rotated value;
a fourth complex adder for accepting the complex value from the input port of the $\pi/4$ complex rotator and the third $\pi/2$ complex rotated value and generating a corresponding fourth complex sum;

five right shifters for respectively shifting the fourth complex sum right by 1 bit, 3 bits, 4 bits, 6 bits and 8 bits to generate respective shifted complex values; and

a fifth complex adder for summing together the shifted complex values to generate the corresponding complex $\pi/4$ rotated value.

[c17] 15. The processor of claim 1 wherein $N=2^{n}$, n mod 3 equals 2, and the output portion further comprises a second BFII serially connected to the second BFI.

[c18] 16. The processor of claim 1 wherein $N=2^{n}$, n mod 3 equals 0, and the output portion further comprises a second BFII serially connected to the second BFI, and a second BFIII serially connected to the second BFII.

[c19] 17. The processor of claim 1 wherein the transform processor is an N-point Decimation in Time Inverse Fast Fourier Transform (DIT IFFT) processor.

[c20] 18. The processor of claim 1 further comprising a reordering circuit, the reordering circuit comprising:

buffering means capable of performing a read operation and a write operation for each pipeline cycle as indicated by the pipeline step-count register;

addressing means for providing a read address and a write address to the buffering means;

address staggering means controlling the addressing means for staggering read and write operations to a memory address in the buffering means by one pipeline cycle as indicated by the pipeline step-count register; and

an address generating means for generating a first address according to the pipeline step-count register, and to provide the first address to the address staggering means.

[c21] 19. The processor of claim 18 wherein the buffering means is a dual-ported random access memory (RAM).

[c22] 20. The processor of claim 19 wherein the addressing means includes a read address port and a write address port of the dual-ported RAM.

[c23] 21. The processor of claim 20 wherein the address staggering means includes a

memory latch connecting the read address port to the write address port, the address latch obtaining a read address from the read address port, and providing the read address to the write address port one pipeline cycle later.

[c24] 22. The processor of claim 18 wherein the reordering circuit further comprises a cycle bit, a cycle bit toggling means that toggles the cycle bit every N pipeline cycles as determined by the pipeline step-count register, and the address generating means generates the first address according to the cycle bit.

[c25] 23. The processor of claim 22 wherein the address generating means includes an address look-up table with entries that provide ordering decoding information.

[c26] 24. The electronic circuit of claim 23 wherein the ordering decoding information contains N entries I_0 to I_{N-1} and for a transformed data point $X1_q$ occurring at time interval $T1_r$ an entry I_r contains the value q.

[c27] 25. The processor of claim 24 wherein the address generating means comprises:
means for obtaining an index derived from the pipeline step-count register to generate from the address look-up table the first address, and to provide the first address to the address staggering means when the cycle bit is in a first state; and
means for generating a second address directly from the pipeline step-count register and providing the second address to the address staggering means when the cycle bit is in a second state.

[c28] 26. The processor of claim 22 wherein the address generating means further comprises:
means for bit-wise reflecting a value derived from the pipeline step-count register to generate the first address, and to provide the first address to the address staggering means when the cycle bit is in a first state; and
means for generating a second address directly from the pipeline step-count register and providing the second address to the address staggering means when the cycle bit is in a second state.

[c29] 27. The processor of claim 18 wherein the buffering means contains no more than N slots for storing N data values to be reordered.

[c30] 28. The processor of claim 18 wherein the reordering circuit accepts the transformed complex numbers from the output portion and generates as output reordered transformed complex numbers.

[c31] 29. The processor of claim 18 where the reordering circuit accepts input non-transformed complex numbers and generates as output reordered non-transformed complex numbers to a BFI.

[c32] 30. An electronic circuit comprising:

a processor for accepting N data points X_0 to X_{N-1} and generating N transformed data points $X1_0$ to $X1_{N-1}$ in a local time interval T1 having time intervals $T1_0$ to $T1_{N-1}$, wherein X_i corresponds to $X1_i$, and for each $X1_j$ occurring at $T1_k$ there occurs at time $T1_j$ an $X1_k$ for $0 \le j \le N-1$ and $0 \le k \le N-1$;

buffering means capable of performing a read operation and a write operation for each pipeline cycle as indicated by a pipeline step-count register that supports N cycles, the buffering means accepting a transformed data point from the processor in each pipeline cycle, the buffering means capable of storing N transformed data points;

addressing means for providing a read address and a write address to the buffering means;

address staggering means controlling the addressing means for staggering read and write operations to a memory address in the buffering means by one pipeline cycle as indicated by the pipeline step-count register; and

an address generating means for generating a first address according to the pipeline step-count register, and providing the first address to the address staggering means.

[c33] 31. The electronic circuit of claim 30 wherein the buffering means is a dual-ported random access memory (RAM).

[c34]

32. The electronic circuit of claim 31 wherein the addressing means includes a

read address port and a write address port of the dual-ported RAM.

[c35] 33. The electronic circuit of claim 32 wherein the address staggering means includes a memory latch connecting the read address port to the write address port, the address latch obtaining a read address from the read address port, and providing the read address to the write address port one pipeline cycle later.

[c36] 34. The electronic circuit of claim 30 further comprising a cycle bit, a cycle bit toggling means that toggles the cycle bit every N pipeline cycles as determined by the pipeline step-count register, and the address generating means generates the first address according to the cycle bit.

[c37] 35. The electronic circuit of claim 34 wherein the address generating means includes an address look-up table with entries that provide ordering decoding information.

[c38] 36. The electronic circuit of claim 35 wherein the ordering decoding information contains N entries I_0 to I_{N-1} and for a transformed data point $X1_q$ occurring at time interval $T1_r$ an entry I_r contains the value q.

[c39] 37. The electronic circuit of claim 36 wherein the address generating means further comprises:

means for obtaining an index derived from the pipeline step-count register to generate from the address look-up table the first address, and to provide the first address to the address staggering means when the cycle bit is in a first state; and

means for generating a second address directly from the pipeline step-count register and providing the second address to the address staggering means when the cycle bit is in a second state.

[c40] 38. The electronic circuit of claim 34 wherein the address generating means further comprises:

means for bit-wise reflecting a value derived from the pipeline step-count register to generate the first address, and to provide the first address to the address staggering means when the cycle bit is in a first state; and

means for generating a second address directly from the pipeline step-count register and providing the second address to the address staggering means when the cycle bit is in a second state.

[c41] 39. The electronic circuit of claim 34 wherein the cycle bit toggling means toggles the cycle bit when the pipeline step-count register obtains a value of N-1.

[c42] 40. The electronic circuit of claim 30 wherein the buffering means contains no more than N slots for storing N data values to be reordered.

[c43] 41. An electronic circuit comprising:
a processor for accepting N data points $X1_0$ to $X1_{N-1}$ in a local time interval T1 having time intervals $T1_0$ to $T1_{N-1}$ and generating N transformed data points X_0 to X_{N-1}, wherein X_i corresponds to $X1_i$, and for each $X1_j$ occurring at $T1_k$ there occurs at time $T1_j$ an $X1_k$ for $0 \leq j \leq N-1$ and $0 \leq k \leq N-1$;
buffering means capable of performing a read operation and a write operation for each pipeline cycle as indicated by a pipeline step-count register that supports N cycles, the buffering means having an input port for accepting the data points $X1_0$ to $X1_{N-1}$ in a local time interval T2 and an output port for providing the data points $X1_0$ to $X1_{N-1}$ in the local timer interval T1 to the processor, the buffering means capable of storing N data points;
addressing means for providing a read address and a write address to the buffering means;
address staggering means controlling the addressing means for staggering read and write operations to a memory address in the buffering means by one pipeline cycle as indicated by the pipeline step-count register; and
an address generating means for generating a first address according to the pipeline step-count register, and providing the first address to the address staggering means.

[c44] 42. The electronic circuit of claim 41 wherein the buffering means is a dual-ported random access memory (RAM).

[c45] 43. The electronic circuit of claim 42 wherein the addressing means includes a read address port and a write address port of the dual-ported RAM.

[c46] 44. The electronic circuit of claim 43 wherein the address staggering means includes a memory latch connecting the read address port to the write address port, the address latch obtaining a read address from the read address port, and providing the read address to the write address port one pipeline cycle later.

[c47] 45. The electronic circuit of claim 41 further comprising a cycle bit, a cycle bit toggling means that toggles the cycle bit every N pipeline cycles as determined by the pipeline step-count register, and the address generating means generates the first address according to the cycle bit.

[c48] 46. The electronic circuit of claim 45 wherein the address generating means includes an address look-up table with entries that provide ordering decoding information.

[c49] 47. The electronic circuit of claim 46 wherein the ordering decoding information contains N entries I_0 to I_{N-1} and for a data point $X1_q$ input into the processor at time interval $T1_r$ an entry I_r contains the value q.

[c50] 48. The electronic circuit of claim 47 wherein the address generating means further comprises:

means for obtaining an index derived from the pipeline step-count register to generate from the address look-up table the first address, and to provide the first address to the address staggering means when the cycle bit is in a first state; and

means for generating a second address directly from the pipeline step-count register and providing the second address to the address staggering means when the cycle bit is in a second state.

[c51] 49. The electronic circuit of claim 45 wherein the address generating means further comprises:

means for bit-wise reflecting a value derived from the pipeline step-count register to generate the first address, and to provide the first address to the

address staggering means when the cycle bit is in a first state; and
means for generating a second address directly from the pipeline step-count register and providing the second address to the address staggering means when the cycle bit is in a second state.

[c52] 50. The electronic circuit of claim 45 wherein the cycle bit toggling means toggles the cycle bit when the pipeline step-count register obtains a value of N-1.

[c53] 51. The electronic circuit of claim 41 wherein the buffering means contains no more than N slots for storing N data values to be reordered.